ABSTRACT OF THE DISCLOSURE

An HNMOS transistor (4) has its drain electrode connected to the gate electrode of an NMOS transistor (21), and a logic circuit voltage (VCC) is applied to the drain electrode of the NMOS transistor (21) through a resistor (32). A ground potential is applied to the source electrode of the NMOS transistor (21). A drain potential (V2) at the NMOS transistor (21) is monitored by an interface circuit (1), for indirectly monitoring a potential (VS). Thus provided is a high voltage integrated circuit for preventing damage to a semiconductor device used for performing bridge rectification of a power line.